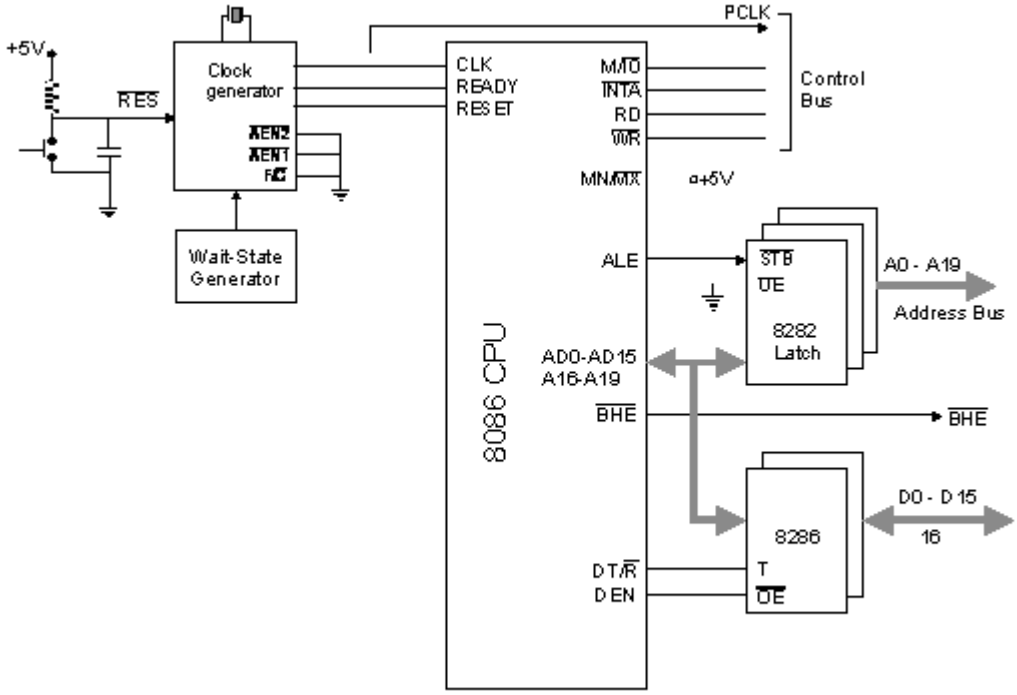
MINIMUM MODE 8086 SYSTEM

- In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN//MX pin to logic 1.

- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.



- The remaining components in the system are latches, Tran receivers, clock generator, memory and I/O devices. Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.

- Latches are generally buffered output D-type flip-flops like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.

- Transreceivers are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals.

- They are controlled by two signals namely, DEN and DT/R.

- The DEN signal indicates the direction of data, i.e. from or to the processor. The system contains memory for the monitor and users program storage.

- Usually, EPROM is used for monitor storage, while RAM for user's program storage. A system may contain I/O devices.

- The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.

- The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

- The read cycle begins in T_1 with the assertion of address latch enable (ALE) signal and also M / IO signal. During the negative going edge of this signal, the valid address is latched on the local bus.

- The BHE and A_0 signals address low, high or both bytes. From T_1 to T_4, the M/IO signal indicates a memory or I/O operation.

- At T_2, the address is removed from the local bus and is sent to the output. The bus is then tristated. The read (RD) control signal is also activated in T_2.

- The read (RD) signal causes the address device to enable its data bus drivers. After RD goes low, the valid data is available on the data bus.

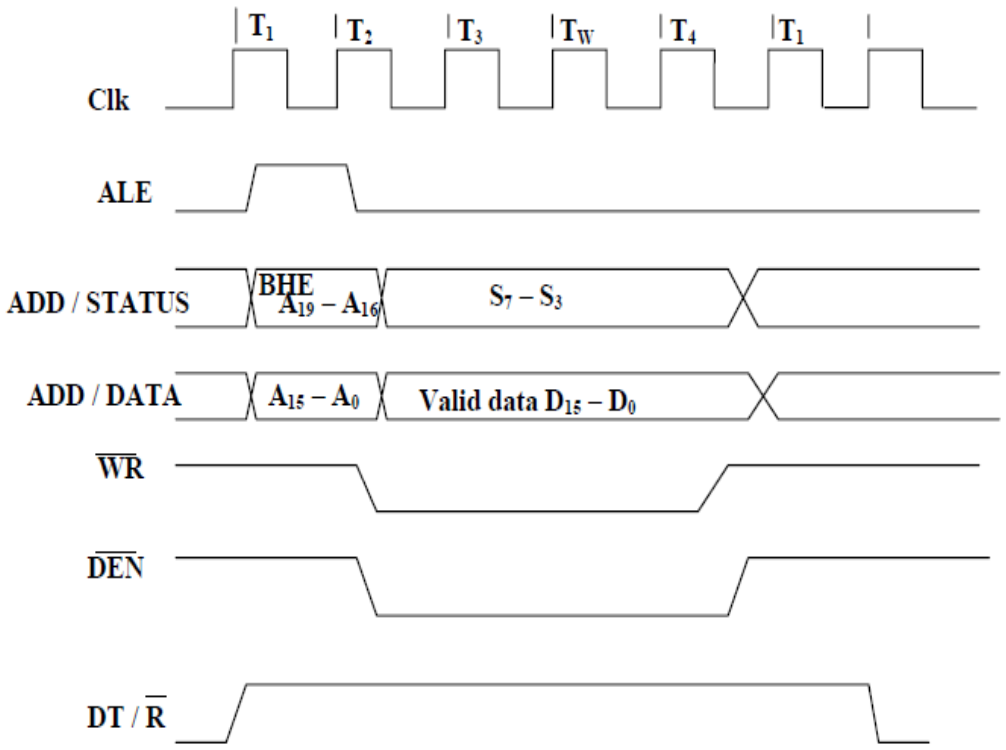
- The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tri state its bus drivers.

- A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal is again asserted to indicate a memory or I/O operation. In T_2, after sending the address in T_1, the processor sends the data to be written to the addressed location.

- The data remains on the bus until middle of T_4 state. The WR becomes active at the beginning of T_2 (unlike RD is somewhat delayed in T_2 to provide time for floating).

- The BHE and A_0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.

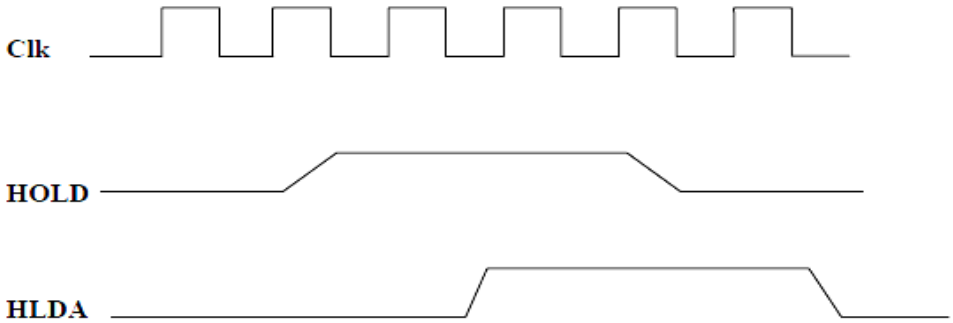
- The M/IO, RD and WR signals indicate the type of data transfer as specified in table below.



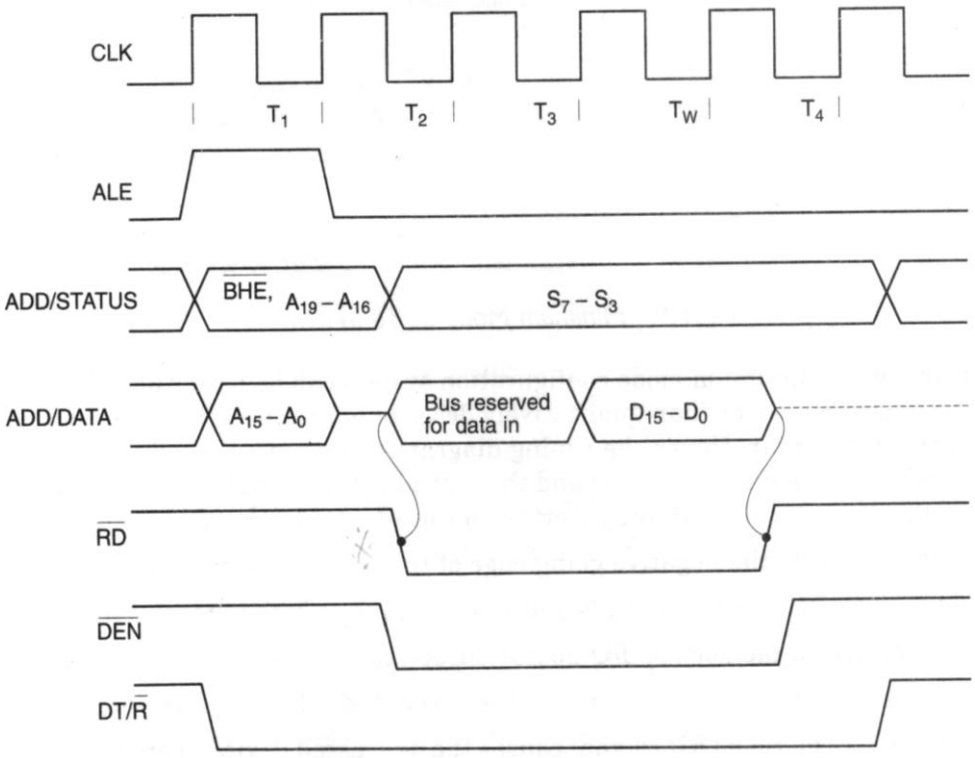
Write Cycle Timing Diagram for Minimum Mode

Hold Response sequence: The HOLD pin is checked at leading edge of each clock pulse. If it is received active by the processor before T_4 of the previous cycle or during T_1 state of the current cycle, the CPU activates HLDA in the next clock cycle and for succeeding bus cycles, the bus will be given to another requesting master.

The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low. When the request is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the next clock.



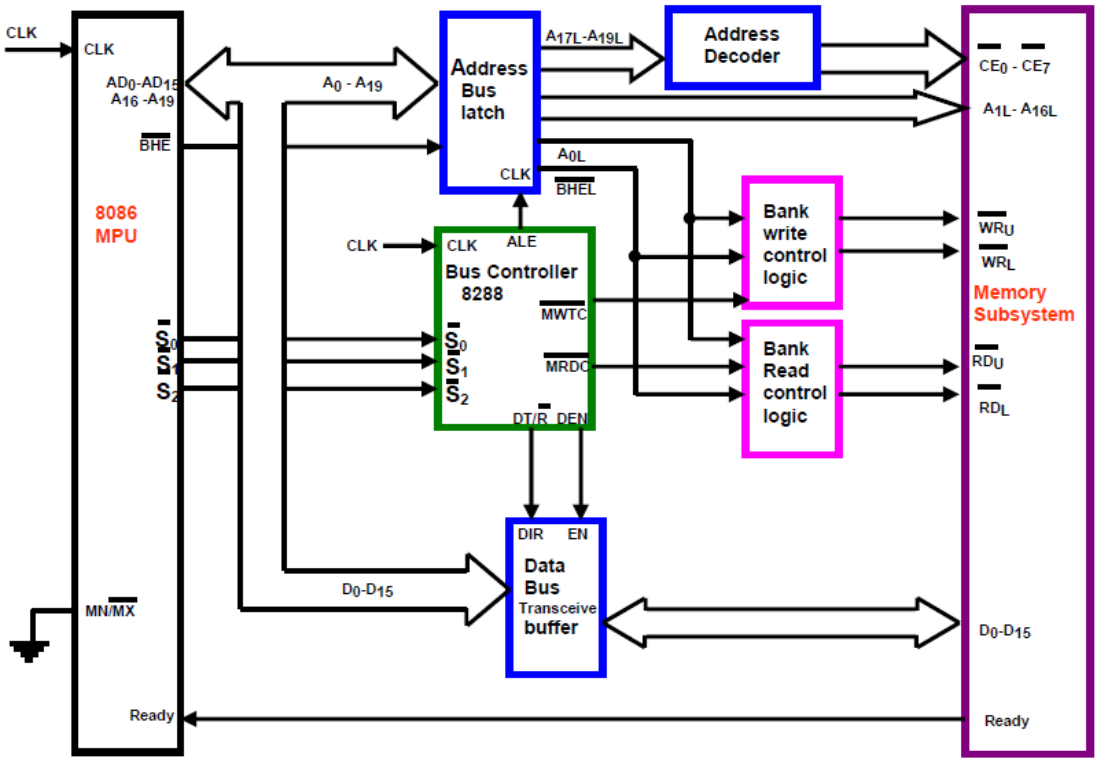
Bus Request and Bus Grant Timings in Minimum Mode System



Read Cycle timing Diagram for Minimum Mode

8086 MAXIMUM MODE

Maximum mode is one of the two hardware modes available to the Intel 8086 and 8088 processors (CPU).Maximum mode is for large applications such as multiprocessing. The mode is hard-wired into the circuit and cannot be changed by software.



The Bus controller is introduced here due to the support of multiprocessor environment of Maximum mode. The decoder is used to select desired memory chips. The remaining components of this circuit are similar to 8088 minimum mode circuit, as shown in figure. Note that the bank high enable signal is used to control the access of even or odd memory banks of 8086 system.

The status codes (S0, S1, S2) of the CPU is used by the bus controller to activate maximum mode memory control signals: These codes are important for multiprocessor environment, supported by Maximum mode.

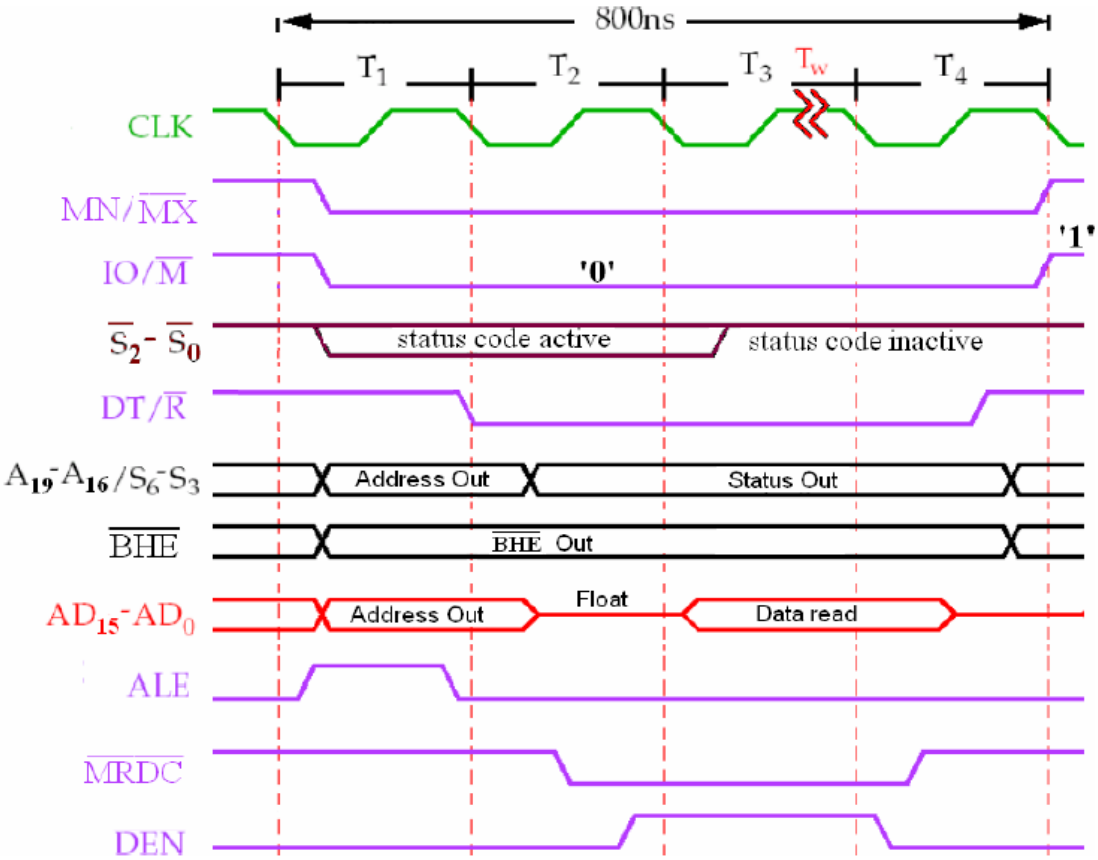
Status Inputs			CPU Cycle	8288 Command
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Maximum-mode Memory-Read bus-cycle of 8086 system

To complete the minimum-mode memory-read bus-cycle, the required control signals with appropriate active logic levels are:

- IO/M = ‘logic 0’, to select memory interface
- MN/MX = ‘logic 0’, to select maximum-mode of operation
- DT/R = ‘logic 0’, to activate the data-receive mode of ‘Data-bus-buffer’
- Valid Physical-address (A0 to A19) and BHE signal is generated by CPU
- ALE-pulse, to latch the valid Physical-address. ( )
- Proper status code S0 to S2 (as shown in table of slide 8) is generated by
- CPU to initiate data reading (MRDC) from the desired memory bank
- DEN = ‘1’, enables the ‘Data-Bus-transceiver-buffer’ to let data pass
- Reset MRDC and DEN signals to END the read-bus-cycle.

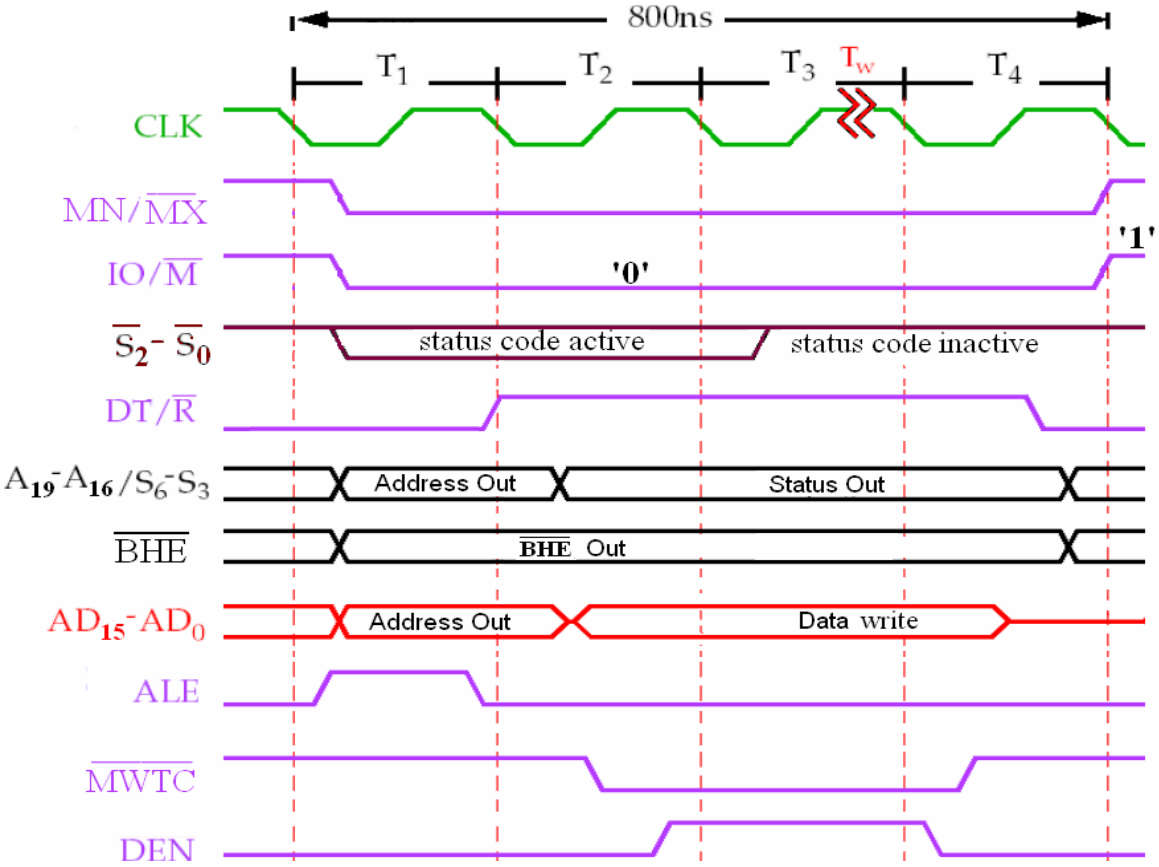
The timing diagram for 8086 maximum mode memory read operation is shown below using logic ‘0’ and ‘1’ waveforms.



Maximum-mode Memory-Read cycle of 8086

The timing diagram for 8086 maximum mode memory read operation is shown below using logic '0' and '1' wave forms.To complete the maximum-mode memory-write bus-cycle, the required control signals with appropriate active logic levels are:

- IO/M = 'logic 0', to select memory interface
- MN/MX = 'logic 0', to select maximum-mode of operation
- DT/R = 'logic 1', to activate the data-transmit mode of 'Data-bus-buffer'
- Valid Physical-address (A0 to A19) and BHE signal is generated by CPU
- ALE-pulse, to latch the valid Physical-address.
- Proper status code S0 to S2 (as shown in table of slide 8) is generated by
- CPU to initiate data writing (MRTC) from the desired memory bank
- DEN = '1', enables the 'Data-Bus-transceiver-buffer' to let data pass
- Reset MRTC and DEN signals to END the read-bus-cycle


800ns
T1
T2
T3
Tw
T4
CLK
MN/MX
'1'
IO/M
'0'
S2- S0
status code active
status code inactive
DT/R
A19-A16/S6-S3
Address Out
Status Out
BHE
BHE Out
AD15-AD0
Address Out
Data write
ALE
MWTC
DEN